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**EE 4550L**

**IC Hardware Security and Trust LAB**

**SPRING 2024**

**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Alex Yeoh**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Alex Yeoh Date: 19th April 2024**

**Report due date: 20th April 2024**

1. **OBJECTIVE**

Implement DES on an FPGA and insert hardware trojans onto the FPGA.

1. **PROCEDURE**

We first loaded the working DES code into the FPGA and verified its functionality. We then modified the DES code before loading it into the FPGA and observed if it would trigger with the default data and key.

I failed to complete part 3 of the lab, as such, that portion of the lab is not present in this procedure section.

1. **RESULT**

Part I:

A screenshot of a computer

Description automatically generated

The DES code successfully compiling.

1. In-System Memory Content Editor with the FPGA programmed with untampered DES.  
   A screenshot of a computer

   Description automatically generated
2. key\_sel.v
3. crp.v
4. 16

Part II:

1. The code is submitted as des\_changed.v
   1. No, 0  
      A screenshot of a computer

      Description automatically generated
2. No, 0  
   A screenshot of a computer

   Description automatically generated
3. Yes, 7  
   A screenshot of a computer

   Description automatically generated

Part III:

Not completed.

1. **CONCLUSION**

My results satisfy the requirements for parts I and II but fail to satisfy the requirements for part III. It would be possible to improve my results by completing part III. I have learned how to implement DES on an FPGA and how to insert a hardware Trojan on it.